AMENDMENT

Claim Amendments

1. (canceled)

2. (canceled)

3. (currently amended) ~~A device of claim 2,~~ A dual gate NMOS device, comprising

a drain,

a source,

a first gate between the drain and the source,

a second gate between the drain and the source, wherein the first gate is closer to the drain and the second gate is closer to the source, and

a lightly doped n-type region having a lower doping level than the drain, extending towards the drain from the gate edge that lies closest to the drain for the first gate, wherein the length of the lightly doped region is between 0.18 μm and 0.5μm and wherein the drain includes a drain silicide and a n+ drain ballasting region extending between the drain silicide and the lightly doped region.

4. (currently amended) A device of claim 3 ~~1~~, wherein the length of the lightly doped region is between 0.18 μm and 0.25 μm.

5. (currently amended) A device of claim 3~~1~~, wherein the lightly doped region extends from the drain to the first gate.

6. (previously presented) A method of reducing soft leakage current degradation in a NMOS snapback device that has at least one gate, a n+ drain and a n+ source, comprising

providing for a n-lightly doped region between the gate and the n+ drain of the device, that has a length substantially the same as the n+ drain depth.

7. (previously presented) A method of claim 6, wherein the n-lightly doped region is formed from an NLDD region by masking a region between the gate and the drain during n+ doping of the drain.

8. (previously presented) A method of claim 7, wherein the n-lightly doped region is formed to extend substantially from the edge of the gate for 0.18 μm – 0.5 μm.

9. (previously presented) A method of claim 8, wherein the n-lightly doped region is formed to extend substantially from the edge of the gate for 0.18 μm – 0.25 μm.,

10. (previously presented) A method of claim 7, wherein the mask may comprise a standard mask used in the process such as n+ composite and silicide exclusion mask.

11. (currently amended) A method of claim 3 ~~1~~, wherein the NMOS device may be a multiple gate device in which the lightly doped region is located between the drain and the gate nearest the drain.